EXHIBIT 1

FILED UNDER SEAL

DDR4 SDRAM

MT40A2G4
MT40A1G8
MT40A512M16

Features

- $V_{DD} = V_{DDQ}$ = 1.2V ±60mV
- V_{PP} = 2.5V, –125mV, +250mV
- On-die, internal, adjustable V_{REFDQ} generation
- 1.2V pseudo open-drain I/O
- Refresh time of 8192-cycle at T_C temperature range:
  – 64ms at -40°C to 85°C
  – 32ms at >85°C to 95°C
  – 16ms at >95°C to 105°C
- 16 internal banks (x4, x8): 4 groups of 4 banks each
- 8 internal banks (x16): 2 groups of 4 banks each
- 8*n*-bit prefetch architecture
- Programmable data strobe preambles
- Data strobe preamble training
- Command/Address latency (CAL)
- Multipurpose register READ and WRITE capability
- Write leveling
- Self refresh mode
- Low-power auto self refresh (LPASR)
- Temperature controlled refresh (TCR)
- Fine granularity refresh
- Self refresh abort
- Maximum power saving
- Output driver calibration
- Nominal, park, and dynamic on-die termination (ODT)
- Data bus inversion (DBI) for data bus
- Command/Address (CA) parity
- Databus write cyclic redundancy check (CRC)
- Per-DRAM addressability
- Connectivity test
- JEDEC JESD-79-4 compliant[2]
- sPPR and hPPR capability
- MBIST-PPR support (Die Revision R only)

Options[1]	Marking
• Configuration	
– 2 Gig x 4	2G4
– 1 Gig x 8	1G8
– 512 Meg x 16	512M16
• 78-ball FBGA package (Pb-free) – x4, x8	
– 9mm x 13.2mm – Rev. A	PM
– 8mm x 12mm – Rev. B, D, G	WE
– 7.5mm x 11mm – Rev. E, H, J, R	SA
• 96-ball FBGA package (Pb-free) – x16	
– 9mm x 14mm – Rev. A	HA
– 8mm x 14mm – Rev. B	JY
– 7.5mm x 13.5mm – Rev. D, E, H	LY
– 7.5mm x 13mm – Rev. J, R	TB
• Timing – cycle time	
– 0.625ns @ CL = 22 (DDR4-3200)	-062E
– 0.682ns @ CL = 21 (DDR4-2933)	-068
– 0.750ns @ CL = 19 (DDR4-2666)	-075
– 0.750ns @ CL = 18 (DDR4-2666)	-075E
– 0.833ns @ CL = 17 (DDR4-2400)	-083
– 0.833ns @ CL = 16 (DDR4-2400)	-083E
– 0.937ns @ CL = 15 (DDR4-2133)	-093E
– 1.071ns @ CL = 13 (DDR4-1866)	-107E
• Operating temperature	
– Commercial (0° ≤ T_C ≤ 95°C)	None
– Industrial (–40° ≤ T_C ≤ 95°C)	IT
– Automotive (–40° ≤ T_C ≤ 105°C)	AT
• Revision	:A, :B, :D, :E, :G, :H, :J, :R

Notes: 1. Not all options listed can be combined to define an offered product. Use the part catalog search on http://www.micron.com for available offerings.
2. Extended temperature mode during temperature controlled refresh is not supported on 8Gb Die Revision R. Refer to Note 2 in Table 18: MR4 Definition.

WRITE Preamble

Programmable WRITE preamble, ^{t}WPRE, can be set to 1^{t}CK or 2^{t}CK via the MR4 register. The 1^{t}CK setting is similar to DDR3. However, when operating in 2^{t}CK WRITE preamble mode, CWL must be programmed to a value at least 1 clock greater than the lowest CWL setting supported in the applicable ^{t}CK range.

Some even settings will require addition of 2 clocks. If the alternate longer CWL was used, the additional clocks will not be required.

READ Preamble

Programmable READ preamble ^{t}RPRE can be set to 1^{t}CK or 2^{t}CK via the MR4 register. Both the 1^{t}CK and 2^{t}CK DDR4 preamble settings are different from that defined for the DDR3 SDRAM. Both DDR4 READ preamble settings may require the memory controller to train (or read level) its data strobe receivers using the READ preamble training.

READ Preamble Training

Programmable READ preamble training can be set to 1^{t}CK or 2^{t}CK. This mode can be used by the memory controller to train or READ level its data strobe receivers.

Temperature-Controlled Refresh

When temperature-controlled refresh mode is enabled, the device may adjust the internal refresh period to be longer than ^{t}REFI of the normal temperature range by skipping external REFRESH commands with the proper gear ratio. For example, the DRAM temperature sensor detected less than 45°C. Normal temperature mode covers the range of -40°C to 85°C, while the extended temperature range covers -40°C to 105°C.

Command Address Latency

COMMAND ADDRESS LATENCY (CAL) is a power savings feature and can be enabled or disabled via the MRS setting. CAL is defined as the delay in clock cycles (^{t}CAL) between a CS_n registered LOW and its corresponding registered command and address. The value of CAL (in clocks) must be programmed into the mode register according to the ^{t}CAL(ns)/^{t}CK(ns) rounding algorithms found in the Converting Time-Based Specifications to Clock-Based Requirements section.

Internal V_{REF} Monitor

This mode enables output of internally generated V_{REFDQ} for monitoring on DQ0, DQ1, DQ2, and DQ3. May be used during V_{REFDQ} training and test. While in this mode, R_{TT} should be set to High-Z. V_{REF_time} must be increased by 10ns if DQ load is 0pF, plus an additional 15ns per pF of loading. This measurement is for verification purposes and is NOT an external voltage supply pin.

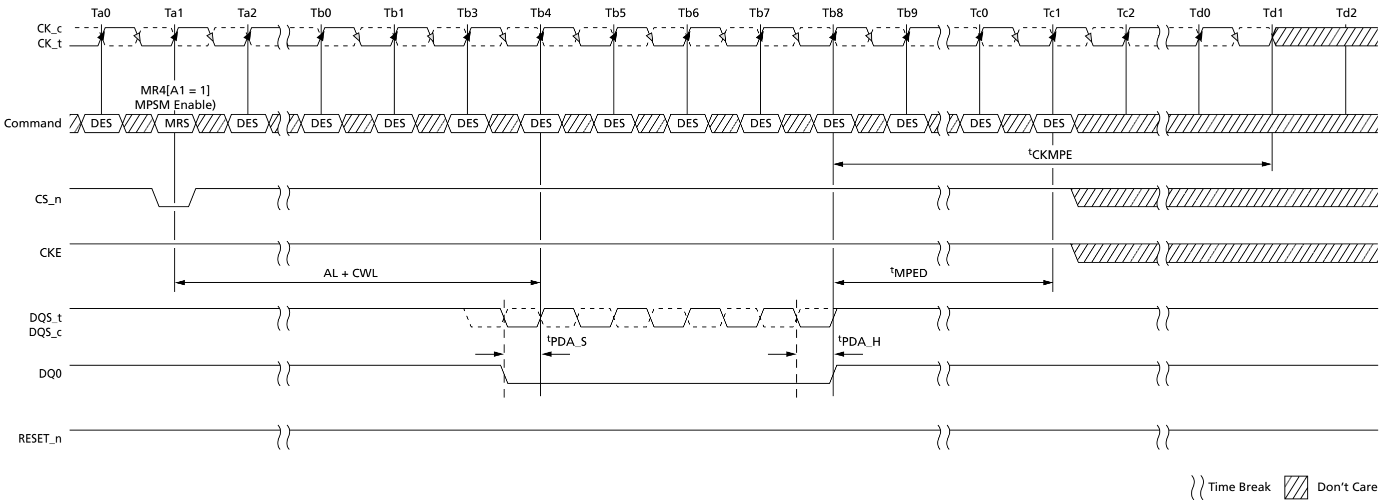
Maximum Power Savings Mode

This mode provides the lowest power mode where data retention is not required. When the device is in the maximum power saving mode, it does not need to guarantee data retention or respond to any external command (except the MAXIMUM POWER SAVING MODE EXIT command and during the assertion of RESET_n signal LOW).

Maximum Power-Saving Mode Entry in PDA

The sequence and timing required for the maximum power-saving mode with the per-DRAM addressability enabled is illustrated in the figure below.

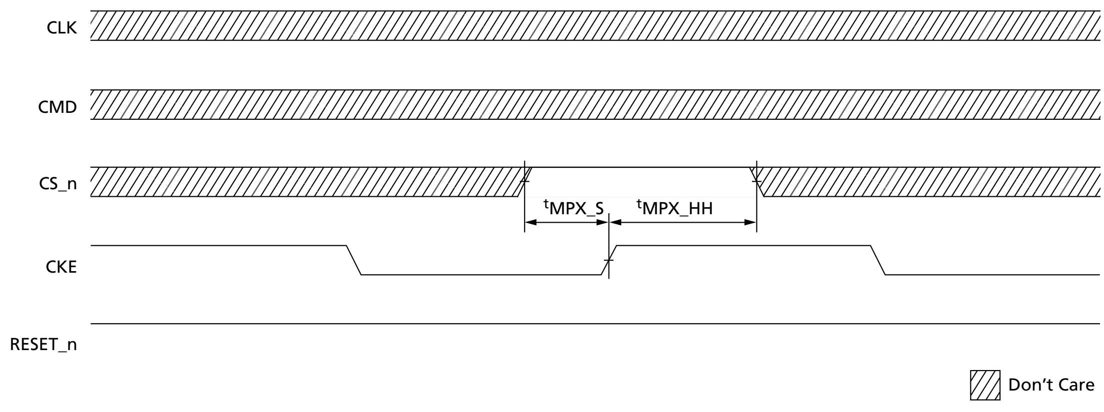
Figure 48: Maximum Power-Saving Mode Entry with PDA



CKE Transition During Maximum Power-Saving Mode

The following figure shows how to maintain maximum power-saving mode even though the CKE input may toggle. To prevent the device from exiting the mode, CS_n should be HIGH at the CKE LOW-to-HIGH edge, with appropriate setup ($^tMPX\_S$) and hold ($^tMPX\_H$) timings.

Figure 49: Maintaining Maximum Power-Saving Mode with CKE Transition



Maximum Power-Saving Mode Exit

To exit the maximum power-saving mode, CS_n should be LOW at the CKE LOW-to-HIGH transition, with appropriate setup ($^tMPX\_S$) and hold ($^tMPX\_LH$) timings, as shown in the figure below. Because the clock receivers (CK_t, CK_c) are disabled during this mode, CS_n = LOW is captured by the rising edge of the CKE signal. If the CS_n signal level is detected LOW, the DRAM clears the maximum power-saving mode MRS bit and begins the exit procedure from this mode. The external clock must be restarted and be stable by ^tCKMPX before the device can exit the maximum power-saving mode. During the exit time (^tXMP), only NOP and DES commands are allowed: NOP during $^tMPX\_LH$ and